Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N/C**
2. **IN A**
3. **GND**
4. **IN B**
5. **N. OUT B**
6. **V +**
7. **N. OUT A**
8. **N.C**

**.075”**

**.083”**

**1**

**2**

**3**

**4**

**8**

**7**

**7**

**6**

**5**

**EL7212**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential:**

**Mask Ref: EL7212**

**APPROVED BY: DK DIE SIZE .075” X .083” DATE: 4/25/22**

**MFG: INTERSIL THICKNESS .026” P/N: EL7212**

**DG 10.1.2**

#### Rev B, 7/1